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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/744,522	01/25/2001	Peter Haas	P00,1963	8561
29177 7590 02/04/2008 BELL, BOYD & LLOYD, LLP P.O. BOX 1135 CHICAGO, IL 60690			EXAMINER PRICE, NATHAN E	
			ART UNIT 2194	PAPER NUMBER
			MAIL DATE 02/04/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/744,522

Applicant(s)

HAAS, PETER

Examiner

Nathan Price

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-13 and 21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-13 and 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
FOR PATENT EXAMINER

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This Office Action is in response to communications received 09 October 2007. Claims 10 – 13 and 21 are pending. Previous objections and rejections not included in this Office Action have been withdrawn.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09 October 2007 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 10 – 13 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 10 – 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Pat. 5,828,884; hereinafter Lee) in view of Sauntry et al. (US 6,349,344 B1; hereinafter Sauntry) and Wold et al. (US Pat. 5,386,568; hereinafter Wold).

5. As to claim 10, Lee teaches a hardware architecture for a core of a processor [col. 6 lines 39 – 41], comprising:

at least one unit for executing one of a logical or arithmetic operation [Fig. 5, processor 510]; and

a data conversion unit for recognizing a type of data and a data address [col. 3 lines 53 – 67], for external data [col. 3 lines 63 – 64], the data conversion unit being arranged to precede the unit for executing a logical or arithmetic operation [col. 3 lines 53 – 67], whereby the data conversion unit recognizes a type of data based upon a type of information accompanying the data address and matches the type of data and the data address before one of an operation is performed or a predetermined type of data is generated in the event of non-match [abstract; col. 3 line 53 – col. 4 line 3].

6. Lee fails to specifically teach an object-oriented data conversion unit. However, Sauntry teaches an object-oriented data conversion unit [col. 3 lines 8 – 16]. It would

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have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because Sauntry teaches that Java components sometimes need to be converted between endian formats [col. 2 lines 18 – 29] and Lee teaches performing the conversion between endian formats [col. 3 lines 53 – 67].

7. Lee fails to specifically teach a divided register as claimed. However, Wold teaches a microprocessor, including at least one register, the at least one register being divided into a first area for indicating the data or object type and into a second area for storing the data or object; wherein an indication of the data type is stored in the first area when loading the piece of data to the register and when performing a logic or arithmetic operation on the data stored in the register, a data conversion is performed by the processor if required based on the indication stored in the register [col. 2 lines 29 – 39; col. 7 lines 3 – 17; col. 9 lines 1 – 19; col. 10 lines 12 – 32]. It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because both address aspects of providing data conversion for processors.

8. As to claim 11, Lee teaches a memory location for the object address and a memory location of a register is respectively divided into a first area and a second area, whereby a type of the object is deposited in the first area [col. 3 line 62 – col. 4 line 3; col. 4 lines 16 – 27; col. 5 lines 60 – 62].

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9. As to claim 12, Lee teaches the object-oriented data conversion unit is arranged to follow the unit executing a logical or an arithmetic operation [col. 3 lines 57 – 62].

10. As to claim 13, Lee teaches the object-oriented data conversion unit is arranged to precede storing of the object in an external storage and a register file [col. 3 lines 57 – 62; col. 5 lines 60 – 62; col. 9 lines 28 – 35].

11. As to claim 21, Lee modified by Wold teaches the processor is configured for automatic index conversion based on the data type stored in the register together with the data when performing indexed addressing [Wold: col. 6 lines 47 – 68; col. 10 lines 12 – 32].

Conclusion

12. The prior art made of record on the P.T.O. 892 that has not been relied upon is considered pertinent to applicant's disclosure. Careful consideration of the cited art is required prior to responding to this Office Action, see 37 C.F.R. 1.111(c).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan Price whose telephone number is (571) 272-4196. The examiner can normally be reached on 6:00am - 2:30pm, Monday - Friday.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on (571) 272-3718. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NP


WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER